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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Allen-Bradley Company Inc
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EXAMINER	
WANG, JIN CHENG	

ART UNIT	PAPER NUMBER
2672	20

DATE MAILED: 08/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/672,639	Applicant(s) DOTSON ET AL./	
	Examiner Jin-Cheng Wang	Art Unit 2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,22-27 and 29-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,22-27 and 29-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/24/2004 has been entered. Claims 30-35 have been newly added. Claims 15-21 and 28 have been canceled. Claims 1 and 22 have been amended. Claims 1-14, 22-27, 29-35 are pending in the application.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tjandrasuwita U.S. Patent No. 6,198,469 (hereinafter Tjandrasuwita) in view of Reddy et al. U.S. Patent No. 6,215,459 (Reddy) and Hannah U.S. Patent No. 5,568,192 (hereinafter Hannah).

3. Claim 1:

(a) Tjandrasuwita teaches a raster engine (flat panel interface 113 of figure 2) for interfacing a frame buffer in a computer system (figure 1) to a plurality of disparate display types over a single interface (e.g., column 4, lines 52-61), comprising:

At least one control register programmable via the computer system to select a display mode (e.g., column 5, lines 58-65, e.g., the display mode can be selected at any given time; see figure 2, and column 6, lines 1-20);

A programmable grayscale generator (e.g., figures 2-4 and column 5, lines 11-67, column 6, lines 1-67, column 8, lines 1-18) to generate grayscale formatted data (e.g., column 3, lines 60-67; column 8, lines 28-35) for a plurality of disparate display types and formats (e.g., Dual Panel Dual Scan Super Twisted Nematic LCD Panels and single STN LCD panels; column 11, lines 15-51) from pixel data in the frame buffer (e.g., column 4, lines 50-67; column 5, lines 1-47), wherein the grayscale generator generates grayscale data according to the selected display mode (e.g., column 5, lines 58-65, the display mode can be selected at any given time; see also figure 2, and column 6, lines 1-20, to generate gray scale shading using time or frame modulation technique and the different gray shades can be generated by turning on and off the pixel; see for example, column 6, lines 48-60); and

A logic device (e.g., multiplexor 208; SEL2 which may originate from a control register that is programmed by the CPU as indicated by the user) adapted to select appropriate pixel data from the grayscale generator (e.g., figures 2-4) in accordance with a selected display mode (see the abstract of the reference), and to provide the selected pixel data to a single output (e.g., figure 2, and column 6, lines 2-20).

(b) However, Tjandrasuwita does not explicitly disclose the claimed limitation that "wherein the single output can provide data to both CRTs and LCDs."

(c) Reddy teaches the claimed limitation that "the single output can provide data to both CRTs and LCDs" (e.g., Reddy Figures 1, 2, 7, column 2-5). It is clear from Reddy's Fig. 1, 2 and 7 that data is provided from a single output from Look-up-Table 103 of Fig. 1, Fig. 2 to both CRTs and LCDs.

(d) It would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided the single output of Reddy from the Tjandrasuwita's device because such a construction would have provided a means driving displays of different types from a single output (Reddy Figures 1 and 2; column 1-5). Moreover, Reddy further discloses a grayscale color lookup and a logic device 157 and 257 and attribute controller in the video controller to create image signals for the display devices and Tjandrasuwita teaches outputs from the display controller can be displayed in CRTs and LCDs (Tjandrasuwita Figure 1). Tjandrasuwita suggests the claim limitation of "a single output that can provide data to both CRTs and LCDs" because Tjandrasuwita teaches in Fig. 1 a single output within the display graphics controller 107 with the same data being sent to the CRTs and LCDs.

It is clear that Reddy teaches a graphics controller having a single output within the graphics controller that can provide data to both CRTs and LCDs and Tjandrasuwita teaches a graphics controller having outputs that can provide data to both CRTs and LCDs. Tjandrasuwita's graphics controller has a single data input and two data ouputs to the LCDs and CRTs. Tjandrasuwita's graphics controller processes the image data

coming from the memory interface, formats the processed data, and passes the same data to the two output data lines, as can be seen in Figure 1. Therefore, there is a single output within the graphics controller of Tjandrasuwita. Moreover, Tjandrasuwita could have incorporated the Reddy's graphics controller to replace its own graphics controller to produce a single output that can provide data to both CRTs and LCDs to provide a single video controller which can control more than one video display having the SAME or COMMON resolution and refresh rate for diverse display devices (Reddy column 3). Although the internal structure of Tjandrasuwita is not described, it is clear from the internal structure of Reddy that Tjandrasuwita's graphics controller has a multitude of blocks similar to Reddy's wherein a single output exists before being separated into two different data paths to be routed to the CRTs and LCDs (See Reddy Figures 1-2 and Tjandrasuwita Fig. 1) to provide a single video controller which can control more than one video display having the same resolution and refresh rate (Reddy column 3).

Tjandrasuwita could also have incorporated the video controller of Reddy to be attached to an output from Tjandrasuwita's integrated processing circuit 101 to provide a single output for the LCDs and CRTs.

(e) Such modification would have been required for portable computers or multimedia presentation wherein the same image is to be displayed on both the LCD and CRT displays (Reddy column 3).

Tjandrasuwita could have incorporated the video controller of Reddy within the Tjandrasuwita's integrated processing circuit 101 to provide a single output for the LCDs and CRTs because such a construction would have provided a means driving displays of different types from a single output (Reddy Figures 1 and 2; column 1-5) to provide a

single video controller which can control more than one video display having the SAME IMAGE resolution and refresh rate (Reddy column 3). Moreover, Reddy further discloses a grayscale color lookup and a logic device 157 and 257 and attribute controller in the video controller to create image signals for the display devices and Tjandrasuwita teaches outputs from the display controller can be displayed in CRTs and LCDs (Tjandrasuwita Figure 1).

Tjandrasuwita could have incorporated the video controller of Reddy to be attached to an output from Tjandrasuwita's integrated processing circuit 101 to provide a single output for the LCDs and CRTs. Such modification would have been required for portable computers or multimedia presentation for DISPLAYING the image having the SAME resolution and refresh rate ON BOTH the LCD and CRT DISPLAYS and SWITCHING IMAGES BETWEEN the LCDs and CRTs from the single output when desired (Reddy column 3).

(f) However, Tjandrasuwita and Reddy is silent to the claim limitation of "a Y Cr Cb encoder".

(g) Hannah teaches a logic system including a pixel shifting logic system (shifting pixel positions in the LUT), Y Cr Cb encoder (for conversion between the RGB color space and YUV color space) (e.g. Hannah column 9).

(h) It would have been obvious to have incorporated Hannah's logic system including a Y Cr Cb decoder into Tjandrasuwita and Reddy's raster engine because Tjandrasuwita teaches a logic system including the multiplexor of Fig. 2 performing the pixel shifting logic operations and DAC of column 5. Reddy teaches a logic system including a LUT, DAC and a pixel shifting logic system because color conversion

involves pixel shifting operations in a color lookup table (Figs. 1-2 and column 2). Tjandrasuwita and Reddy is only silent to a Y Cr Cb encoder. Therefore, Tjandrasuwita and Reddy could have incorporated Hannah's color conversion scheme in LUT for converting the RGB color data to Y Cr Cb data (Hannah column 9, Reddy column 2).

(i) One of ordinary skill in the art could have been motivated to do this to provide planar pixel data which are suitable for processing into compressed video bit streams (Hannah column 3).

Claim 2:

The claim 2 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of a grayscale look up table control register programmable by the computer system. However, the Tjandrasuwita reference further discloses the claimed limitation of a grayscale look up table control register programmable by the computer system (i.e., the dithering engine 204 of figure 2, and the mapping scheme may be designed to be programmable as well, column 7, lines 60-67).

Claim 3:

The claim 3 encompasses the same scope of invention as that of claim 2 except additional claimed limitation of the grayscale look up table comprising a three dimensional matrix having a frame dimension (column 11, lines 52-67, e.g., FPFC[3:0]), a vertical dimension (FPVC[3:0]), a horizontal dimension (FPHC[3:0]), and a plurality of data entries associated with each combination of frame, vertical, and horizontal dimensions, and wherein the data entries comprise a plurality of matrix position enable

bits adapted to indicate whether a pixel in the display is energized (column 9, lines 43-62).

Claim 4:

The claim 4 encompasses the same scope of invention as that of claim 3 except additional claimed limitation of the grayscale generator further comprising a frame counter, a vertical counter, and a horizontal counter, and wherein the grayscale look up table data entries define dithering operation for a pixel value according to the frame counter, the vertical counter, and the horizontal counter. However, the Tjandrasuwita reference further discloses the claimed limitation of the grayscale generator (e.g., figures 2-4 and column 5, lines 11-67, column 6, lines 1-67, column 8, lines 1-18) further comprising a frame counter, a vertical counter, and a horizontal counter (column 2, lines 47-62), and wherein the grayscale look up table data entries (Table 1 of column 7) define dithering operation for a pixel value according to the frame counter, the vertical counter, and the horizontal counter (column 2, lines 47-62).

Claim 5:

The claim 5 encompasses the same scope of invention as that of claim 4 except additional claimed limitation of the frame dimension comprising one of 3 and 4, wherein the vertical dimension comprises one of 3 and 4, and wherein the horizontal dimension comprises one of 3 and 4. However, the Tjandrasuwita reference further discloses the claimed limitation of the frame dimension (FPFC[3:0], see also column 9, line 64), wherein the vertical dimension comprises one of 3 and 4 (FPVC[3:0], column 9, line 57), wherein the horizontal dimension comprises one of 3 and 4 (FPHC[3:0], column 9, line 58).

Claim 6:

The claim 6 encompasses the same scope of invention as that of claim 5 except additional claimed limitation of the grayscale generator adapted to translate 3 bits of pixel data for a pixel in the display to generate grayscale formatted data for the pixel to provide 8 shades of gray according to the selected display mode and the grayscale lookup table data entries. However, the Tjandrasuwita reference further discloses the claimed limitation of the grayscale generator (e.g., figures 2-4 and column 5, lines 11-67, column 6, lines 1-67, column 8, lines 1-18) adapted to translate 3 bits of pixel data for a pixel in the display to generate grayscale formatted data for the pixel to provide 8 shades of gray according to the selected display mode (column 8, lines 3-18) and the grayscale lookup table data entries (Table 1 of column 7). It is noted that in the two-to-one mapping of the mapping of 16 possible gray-level inputs to 8 gray-levels, wherein the 4 bits of pixel data can be translated into 3 bits (Table 1 of column 7).

Claims 7-8:

Claims 7-8 is a rephrasing of claims 5-6 in a method form. The claim is rejected for the same reason as set forth in claims 5-6.

Claim 9:

Claim 9 is a rephrasing of claim 4 in a method form. The claim is rejected for the same reason as set forth in claim 4.

Claim 10:

The claim 10 encompasses the same scope of invention as that of claim 6 except additional claimed limitation of the grayscale generator programmable by a user via an application program in the computer system. However, the Tjandrasuwita reference

further discloses the claimed limitation of the grayscale generator (e.g., figures 2-4 and column 5, lines 11-67, column 6, lines 1-67, column 8, lines 1-18) programmable by a user via an application program in the computer system, e.g., the apparatus generates gray scale shading data in response to input color data that is programmable (see the abstract of the reference and column 4, lines 1-61 of the specification).

Claim 11:

The claim 11 encompasses the same scope of invention as that of claim 10 except additional claimed limitation of the application program being a video driver. However, the Tjandrasuwita reference further discloses the claimed limitation of the application program being a video driver (column 4, lines 9-61). The Office interprets the integrated processor circuit 101 as a video driver.

Claim 12:

Claim 12 is a rephrasing of claim 10 in a method form. The claim is rejected for the same reason as set forth in claim 10.

Claim 13:

The claim 13 encompasses the same scope of invention as that of claim 6 except additional claimed limitation of the display type. However, the Tjandrasuwita reference further discloses the claimed limitation of the display type (column 4, lines 52-61).

Claim 14:

Claim 14 is a rephrasing of claim 13 in a method form. The claim is rejected for the same reason as set forth in claim 13.

4. Claims 22-27, 30-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tjandrasuwita U.S. Patent No. 6,198,469 (hereinafter Tjandrasuwita) in view of Reddy et al. U.S. Patent No. 6,215,459 (Reddy) and Dye U.S. Patent No. 4,965,559 (hereinafter Dye).

5. Claim 22:

(a) The Tjandrasuwita reference has taught a raster engine (i.e., the flat panel interface 113 of figure 2) for interfacing a frame buffer in a computer system to one of a plurality of disparate display types (e.g., column 4, lines 52-61), comprising:

Means for selecting a display mode (e.g., the mode selecting circuit 403, see also column 5, lines 58-65);

Means for obtaining pixel data from the frame buffer (e.g., figure 1 and column 4) and programmable (e.g., the dithering engine 204 and the mapping scheme of column 7 may be designed to be programmable as well, see also column 8, lines 3-67) via the computer system to generate grayscale formatted data for a plurality of disparate display types and formats including the selected display mode (e.g., Dual Panel Dual Scan Super Twisted Nematic LCD Panels and single STN LCD panels; column 11, lines 15-51; see also column 5, lines 58-65, the display mode can be selected at any given time; see also figure 2, and column 6, lines 1-20, to generate gray scale shading using time or frame modulation technique and the different gray shades can be generated by turning on and off the pixel; see for example, column 6, lines 48-60); and

A parallel output means (e.g., multiplexor 208 having a parallel output) for selecting appropriate pixel data from the means for obtaining pixel data for the selected

display mode (e.g., figures 2-4), and for providing the selected pixel data at a single parallel output according to the selected display mode (e.g., figure 2, and column 6, lines 2-20).

(b) However, Tjandrasuwita does not explicitly disclose the claimed limitation that "wherein the single output can provide data to both CRTs and LCDs."

(c) Reddy teaches the claimed limitation that "the single output can provide data to both CRTs and LCDs" (e.g., Reddy Figures 1, 2, 7, column 2-5). It is clear from Reddy's Fig. 1, 2 and 7 that data is provided from a single output from Look-up-Table 103 of Fig. 1, Fig. 2 to both CRTs and LCDs.

(d) It would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided the single output of Reddy from the Tjandrasuwita's device because such a construction would have provided a means driving displays of different types from a single output (Reddy Figures 1 and 2; column 1-5). Moreover, Reddy further discloses a grayscale color lookup and a logic device 157 and 257 and attribute controller in the video controller to create image signals for the display devices and Tjandrasuwita teaches outputs from the display controller can be displayed in CRTs and LCDs (Tjandrasuwita Figure 1). Tjandrasuwita suggests the claim limitation of "a single output that can provide data to both CRTs and LCDs" because Tjandrasuwita teaches in Fig. 1 a single output within the display graphics controller 107 with the same data being sent to the CRTs and LCDs.

It is clear that Reddy teaches a graphics controller having a single output within the graphics controller that can provide data to both CRTs and LCDs and Tjandrasuwita

teaches a graphics controller having outputs that can provide data to both CRTs and LCDs. Tjandrasuwita's graphics controller has a single data input and two data ouputs to the LCDs and CRTs. Tjandrasuwita's graphics controller processes the image data coming from the memory interface, formats the processed data, and passes the same data to the two output data lines, as can be seen in Figure 1. Therefore, there is a single output within the graphics controller of Tjandrasuwita. Moreover, Tjandrasuwita could have incorporated the Reddy's graphics controller to replace its own graphics controller to produce a single output that can provide data to both CRTs and LCDs to provide a single video controller which can control more than one video display having the SAME or COMMON resolution and refresh rate for diverse display devices (Reddy column 3). Although the internal structure of Tjandrasuwita is not described, it is clear from the internal structure of Reddy that Tjandrasuwita's graphics controller has a multitude of blocks similar to Reddy's wherein a single output exists before being separated into two different data paths to be routed to the CRTs and LCDs (See Reddy Figures 1-2 and Tjandrasuwita Fig. 1) to provide a single video controller which can control more than one video display having the same resolution and refresh rate (Reddy column 3).

Tjandrasuwita could also have incorporated the video controller of Reddy to be attached to an output from Tjandrasuwita's integrated processing circuit 101 to provide a single output for the LCDs and CRTs.

(e) Such modification would have been required for portable computers or multimedia presentation wherein the same image is to be displayed on both the LCD and CRT displays (Reddy column 3).

Tjandrasuwita could have incorporated the video controller of Reddy within the Tjandrasuwita's integrated processing circuit 101 to provide a single output for the LCDs and CRTs because such a construction would have provided a means driving displays of different types from a single output (Reddy Figures 1 and 2; column 1-5) to provide a single video controller which can control more than one video display having the SAME IMAGE resolution and refresh rate (Reddy column 3). Moreover, Reddy further discloses a grayscale color lookup and a logic device 157 and 257 and attribute controller in the video controller to create image signals for the display devices and Tjandrasuwita teaches outputs from the display controller can be displayed in CRTs and LCDs (Tjandrasuwita Figure 1).

Tjandrasuwita could have incorporated the video controller of Reddy to be attached to an output from Tjandrasuwita's integrated processing circuit 101 to provide a single output for the LCDs and CRTs. Such modification would have been required for portable computers or multimedia presentation for DISPLAYING the image having the SAME resolution and refresh rate ON BOTH the LCD and CRT DISPLAYS and SWITCHING IMAGES BETWEEN the LCDs and CRTs from the single output when desired (Reddy column 3).

(f) However, Tjandrasuwita and Reddy is silent to the claim limitation of "means for buffering data transferred from the frame buffer to eliminate or reduce data underflow".

(g) Dye teaches means for buffering data transferred from the frame buffer to eliminate or reduce data underflow (*e.g., Dye teaches a dual port RAM/DRAM and an interrupter for buffering data transferred from the frame buffer or the display RAM to*

produce control logic or instructions for bit level operations and control logic and thereby reducing data underflow in bit level operations; Dye column 3-4).

(h) It would have been obvious to have incorporated Dye's dual port RAM/DRAM into Tjandrasuwita and Reddy's raster engine because Tjandrasuwita teaches a logic system including the multiplexor of Fig. 2 capable of display mode selection and Dye teaches a configuration logic control in Fig. 3 capable of display mode selection.

(i) One of ordinary skill in the art could have been motivated to do this to provide memory ports for data interface to provide bit level operations, e.g., during a shift register load cycle, for controlling a variety of display activities (Dye column 3-4) and for selecting pixel data for displaying (Dye column 2).

Claim 23-25:

The claim limitation as recited in each of the claims 23-25 encompasses the same scope of invention as that of the claims 3 and 4 in except additional claim limitation of "the grayscale look up table control register". However, Tjandrasuwita further discloses the claim limitation of a grayscale look up table control register programmable by a computer system (e.g., the dithering engine 204 and the mapping scheme of column 7 may be designed to be programmable as well, and see also column 8, lines 3-67).

Claim 26:

The claim limitation as recited in the claim 26 encompasses the same scope of invention as that of claim 6. The claim is rejected for the same reason as set forth respectively in claim 6.

Claim 27:

The claim limitation as recited in the claim 27 encompasses the same scope of invention as that of claim 5. The claim is rejected for the same reason as set forth respectively in claim 5.

Claim 30:

Dye further discloses the claim limitation of the pixel shifting logic system receiving pixel data from a multiplexer and presenting the selected pixel data at a parallel output in accordance with the selected display mode (*Dye discloses a configuration logic system in Fig. 3 receiving pixel data from a multiplexer such as digital video multiplexer through a P2 connector and presenting the selected pixel data at the parallel output to the look-up table in accordance with the selected display mode; Fig. 3 and column 2-4*).

Claim 31:

Dye further discloses the claim limitation of an underflow system that buffers data transferred to the grayscale generator from the frame buffer to eliminate or reduce data underflow conditions (*e.g., Dye teaches a dual port RAM/DRAM and an interrupter for buffering data transferred from the frame buffer or the display RAM to produce control logic or instructions for bit level operations and control logic and thereby reducing data underflow in bit level operations; Dye column 3-4*).

Claim 32:

Dye further discloses the claim limitation of a dual port RAM device and a pixel multiplexer that selects pixel data from the dual port RAM device according to a selected display mode (e.g., *Dye discloses in Fig. 3 a dual port RAM device and a configuration logic which acts as a pixel multiplexer that selects pixel data through a bus from the dual port RAM device according to a selected display mode for one of the four display types as shown; see also column 2-4*).

Claim 33:

Dye further discloses the claim limitation of the underflow system generating an interrupt based on a detected or predicted underflow condition (e.g., *Dye discloses a VME interrupter generating interrupts on any of seven VME bus interrupt levels and supplies a 16-bit vector when VME interrupt handler responses with a valid interrupt acknowledge cycle and thereby detecting an underflow condition based on the interrupt levels; see Dye column 2-4*).

Claim 34:

Dye further discloses the claim limitation of a host processor receiving the generated interrupt and balancing bus load and/or limiting burst sizes to reduce or minimize undesirable visual effects associate with a starved or empty raster engine (e.g., *Dye discloses a microprocessor with instruction set containing screen control logic, DRAM and VRAM control logic, host interface logic, bit level arithmetic and logic operations performing for example refresh cycles as well as all display functions and allowing video data to be shifted to refresh the screen. The control logic and instructions minimize undesirable visual effects associated with an empty raster engine at certain time intervals of the video cycle; Dye column 2-4*).

Claim 35:

Dye further discloses the claim limitation of a video stream signature analyzer to enable self-testing (e.g., *Dye discloses a local controller including a microprocessor capable of a diagnostic testing; column 2-4*).

6. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tjandrasuwita U.S. Patent No. 6,198,469 (hereinafter Tjandrasuwita) in view of Reddy et al. U.S. Patent No. 6,215,459 (Reddy), Hannah U.S. Patent No. 5,568,192 (hereinafter Hannah) and Dye U.S. Patent No. 4,965,559 (hereinafter Dye).

Claim 29:

(a) The claim limitation as recited in the claim 29 encompasses the same scope of invention as that of claim 22 except additional claim limitation of "the output device comprising two or more of a pixel shifting logic system, a YcrCb encoder, and a DAC".

(b) Tjandrasuwita, Reddy and Dye is silent to the claim limitation of "a YcrCb encoder"

(c) Hannah teaches a logic system including a pixel shifting logic system (shifting pixel positions in the LUT), Y Cr Cb encoder (for conversion between the RGB color space and YUV color space) (e.g. Hannah column 9).

(d) It would have been obvious to have incorporated Hannah's logic system into Tjandrasuwita, Reddy and Dye's raster engine because Tjandrasuwita teaches a logic system including the multiplexor of Fig. 2 performing the pixel shifting logic operations and DAC of column 5. Reddy teaches a logic system including a LUT, DAC and a pixel

shifting logic system because color conversion involves pixel shifting operations in a color lookup table (Figs. 1-2 and column 2). Tjandrasuwita and Reddy is only silent to a Y Cr Cb encoder. Therefore, Tjandrasuwita and Reddy could have incorporated Hannah's color conversion scheme in LUT for converting the RGB color data to Y Cr Cb data (Hannah column 9, Reddy column 2).

(e) One of ordinary skill in the art could have been motivated to do this to provide planar pixel data which are suitable for processing into compressed video bit streams (Hannah column 3).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jin-Cheng Wang whose telephone number is (703) 605-1213. The examiner can normally be reached on 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Razavi can be reached on (703) 305-4713. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-6606 for regular communications and (703) 308-6606 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 395-3900.

JEFFERY BRIER
PRIMARY EXAMINER

jcw
July 29, 2004